1-12-00

Practitioner's Docket No. 460-009131-US(PAR) **PATENT** A

Preliminary Classification:
Proposed Class:
Subclass:
NOTE: *"All applicants are requested to include a preliminary classification on newly filed patent applications. The preliminary classification, preferably class and subclass designations, should be identified in the upper right-hand corner of the letter of transmittal accompanying the application papers, for example 'Proposed Class 2, subclass 129.' " M.P.E.P. § 601, 7th ed.*

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Box Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

NEW APPLICATION TRANSMITTAL

Transmitted herewith for filing is the patent application of
Inventor(s): Matti FLOMAN, Ari AHO, Markku LIPPONEN, Mikko SILTANEN

WARNING: *37 C.F.R. § 1.41(a)(1) points out:*

"(a) A patent is applied for in the name or names of the actual inventor or inventors.

"(1) The inventorship of a nonprovisional application is that inventorship set forth in the oath or declaration as prescribed by § 1.63, except as provided for in § 1.53(d)(4) and § 1.63(d). If an oath or declaration as prescribed by § 1.63 is not filed during the pendency of a nonprovisional application, the inventorship is that inventorship set forth in the application papers filed pursuant to § 1.53(b), unless a petition under this paragraph accompanied by the fee set forth in § 1.17(i) is filed supplying or changing the name or names of the inventor or inventors."

For (title):

METHOD FOR REFRESHING A DYNAMIC MEMORY

CERTIFICATION UNDER 37 C.F.R. § 1.10*
(Express Mail label number is mandatory.)
(Express Mail certification is optional.)

I hereby certify that this New Application Transmittal and the documents referred to as attached therein are being deposited with the United States Postal Service on this date January 11, 2000, in an envelope as "Express Mail Post Office to Addressee," mailing Label Number EL067144474US, addressed to the: Assistant Commissioner for Patents, Washington, D.C. 20231.

Elaine Mian
(type or print name of person mailing paper)

Elaine Mian
Signature of person mailing paper

WARNING: *Certificate of mailing (first class) or facsimile transmission procedures of 37 C.F.R. § 1.8 cannot be used to obtain a date of mailing or transmission for this correspondence.*

***WARNING:** Each paper or fee filed by "Express Mail" **must** have the number of the "Express Mail" mailing label placed thereon prior to mailing. 37 C.F.R. § 1.10(b).*
*"Since the filing of correspondence under § 1.10 without the Express Mail mailing label thereon is an oversight that can be avoided by the exercise of reasonable care, requests for waiver of this requirement will **not** be granted on petition." Notice of Oct. 24, 1996, 60 Fed. Reg. 56,439, at 56,442.*

1. Type of Application

This new application is for a(n)

(check one applicable item below)

☒ Original (nonprovisional)

☐ Design

☐ Plant

WARNING: ***Do not*** *use this transmittal for a completion in the U.S. of an International Application under 35 U.S.C. § 371(c)(4), unless the International Application is being filed as a divisional, continuation or continuation-in-part application.*

WARNING: ***Do not*** *use this transmittal for the filing of a provisional application.*

NOTE: If one of the following 3 items apply, then complete and attach ADDED PAGES FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF A PRIOR U.S. APPLICATION CLAIMED and a NOTIFICATION IN PARENT APPLICATION OF THE FILING OF THIS CONTINUATION APPLICATION.

☐ Divisional.

☐ Continuation.

☐ Continuation-in-part (C-I-P).

2. Benefit of Prior U.S. Application(s) (35 U.S.C. §§ 119(e), 120, or 121)

NOTE: A nonprovisional application may claim an invention disclosed in one or more prior filed copending nonprovisional applications or copending international applications designating the United States of America. In order for a nonprovisional application to claim the benefit of a prior filed copending nonprovisional application or copending international application designating the United States of America, each prior application must name as an inventor at least one inventor named in the later filed nonprovisional application and disclose the named inventor's invention claimed in at least one claim of the later filed nonprovisional application in the manner provided by the first paragraph of 35 U.S.C. § 112. Each prior application must also be:

(i) An international application entitled to a filing date in accordance with PCT Article 11 and designating the United States of America; or

(ii) Complete as set forth in § 1.51(b); or

(iii) Entitled to a filing date as set forth in § 1.53(b) or § 1.53(d) and include the basic filing fee set forth in § 1.16; or

(iv) Entitled to a filing date as set forth in § 1.53(b) and have paid therein the processing and retention fee set forth in § 1.21(l) within the time period set forth in § 1.53(f).

37 C.F.R. § 1.78(a)(1).

NOTE: If the new application being transmitted is a divisional, continuation or a continuation-in-part of a parent case, or where the parent case is an International Application which designated the U.S., or benefit of a prior provisional application is claimed, then check the following item and complete and attach ADDED PAGES FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF PRIOR U.S. APPLICATION(S) CLAIMED.

WARNING: *If an application claims the benefit of the filing date of an earlier filed application under 35 U.S.C. §§ 120, 121 or 365(c), the 20-year term of that application will be based upon the filing date of the earliest U.S. application that the application makes reference to under 35 U.S.C. §§ 120, 121 or 365(c). (35 U.S.C. § 154(a)(2) does not take into account, for the determination of the patent term, any application on which priority is claimed under 35 U.S.C. §§ 119, 365(a) or 365(b).) For a c-i-p application, applicant should review whether any claim in the patent that will issue is supported by an earlier application and, if not, the applicant should consider canceling the reference to the earlier filed application. The term of a patent is not based on a claim-by-claim approach. See Notice of April 14, 1995, 60 Fed. Reg. 20,195, at 20,205.*

WARNING: *When the last day of pendency of a provisional application falls on a Saturday, Sunday, or Federal holiday within the District of Columbia, any nonprovisional application claiming benefit of the provisional application must be filed prior to the Saturday, Sunday, or Federal holiday within the District of Columbia. See 37 C.F.R. § 1.78(a)(3).*

☐ The new application being transmitted claims the benefit of prior U.S. application(s). Enclosed are ADDED PAGES FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF PRIOR U.S. APPLICATION(S) CLAIMED.

3. Papers Enclosed

A. Required for filing date under 37 C.F.R. § 1.53(b) (Regular) or 37 C.F.R. § 1.153 (Design) Application

15 Pages of specification

2 Pages of claims

2 Sheets of drawing

WARNING: ***DO NOT*** *submit original drawings. A high quality copy of the drawings should be supplied when filing a patent application. The drawings that are submitted to the Office must be on strong, white, smooth, and non-shiny paper and meet the standards according to § 1.84. If corrections to the drawings are necessary, they should be made to the original drawing and a high-quality copy of the corrected original drawing then submitted to the Office. Only one copy is required or desired. For comments on proposed then-new 37 C.F.R. § 1.84, see Notice of March 9, 1988 (1990 O.G. 57-62).*

NOTE: *"Identifying indicia, if provided, should include the application number or the title of the invention, inventor's name, docket number (if any), and the name and telephone number of a person to call if the Office is unable to match the drawings to the proper application. This information should be placed on the back of each sheet of drawing a minimum distance of 1.5 cm. (5/8 inch) down from the top of the page . . ." 37 C.F.R. § 1.84(c)).*

(complete the following, if applicable)

☐ The enclosed drawing(s) are photograph(s), and there is also attached a "PETITION TO ACCEPT PHOTOGRAPH(S) AS DRAWING(S)." 37 C.F.R. § 1.84(b).

☐ formal

☐ informal

B. Other Papers Enclosed

6 Pages of declaration and power of attorney

1 Pages of abstract

____ Other

4. Additional papers enclosed

☐ Amendment to claims

☐ Cancel in this applications claims _____ before calculating the filing fee. (At least one original independent claim must be retained for filing purposes.)

☐ Add the claims shown on the attached amendment. (Claims added have been numbered consecutively following the highest numbered original claims.)

☒ Preliminary Amendment

☒ Information Disclosure Statement (37 C.F.R. § 1.98)

☒ Form PTO–1449 (PTO/SB/08A and 08B)

☒ Citations

☐ Declaration of Biological Deposit

☐ Submission of "Sequence Listing," computer readable copy and/or amendment pertaining thereto for biotechnology invention containing nucleotide and/or amino acid sequence.

☐ Authorization of Attorney(s) to Accept and Follow Instructions from Representative

☐ Special Comments

☐ Other

5. Declaration or oath (including power of attorney)

NOTE: A newly executed declaration is not required in a continuation or divisional application provided that the prior nonprovisional application contained a declaration as required, the application being filed is by all or fewer than all the inventors named in the prior application, there is no new matter in the application being filed, and a copy of the executed declaration filed in the prior application (showing the signature or an indication thereon that it was signed) is submitted. The copy must be accompanied by a statement requesting deletion of the names of person(s) who are not inventors of the application being filed. If the declaration in the prior application was filed under § 1.47, then a copy of that declaration must be filed accompanied by a copy of the decision granting § 1.47 status or, if a nonsigning person under § 1.47 has subsequently joined in a prior application, then a copy of the subsequently executed declaration must be filed. See 37 C.F.R. §§ 1.63(d)(1)–(3).

NOTE: A declaration filed to complete an application must be executed, identify the specification to which it is directed, identify each inventor by full name including family name and at least one given name, without abbreviation together with any other given name or initial, and the residence, post office address and country or citizenship of each inventor, and state whether the inventor is a sole or joint inventor. 37 C.F.R. § 1.63(a)(1)–(4).

☒ Enclosed

Executed by

(check **all** *applicable boxes)*

☒ inventor(s).

☐ legal representative of inventor(s). 37 C.F.R. §§ 1.42 or 1.43.

☐ joint inventor or person showing a proprietary interest on behalf of inventor who refused to sign or cannot be reached.

☐ This is the petition required by 37 C.F.R. § 1.47 and the statement required by 37 C.F.R. § 1.47 is also attached. See item 13 below for fee.

☐ Not Enclosed.

NOTE: Where the filing is a completion in the U.S. of an International Application or where the completion of the U.S. application contains subject matter in addition to the International Application, the application may be treated as a continuation or continuation-in-part, as the case may be, utilizing ADDED PAGE FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF PRIOR U.S. APPLICATION CLAIMED.

☐ Application is made by a person authorized under 37 C.F.R. § 1.41(c) on behalf of *all* the above named inventor(s).

(The declaration or oath, along with the surcharge required by 37 C.F.R. § 1.16(e) can be filed subsequently).

☐ Showing that the filing is authorized. *(not required unless called into question. 37 C.F.R. § 1.41(d))*

6. Inventorship Statement

WARNING: *If the named inventors are each not the inventors of all the claims an explanation, including the ownership of the various claims at the time the last claimed invention was made, should be submitted.*

The inventorship for all the claims in this application are:

☐ The same.

or

☐ Not the same. An explanation, including the ownership of the various claims at the time the last claimed invention was made,

☐ is submitted.

☐ will be submitted.

7. Language

NOTE: An application including a signed oath or declaration may be filed in a language other than English. An English translation of the non-English language application and the processing fee of $130.00 required by 37 C.F.R. § 1.17(k) is required to be filed with the application, or within such time as may be set by the Office. 37 C.F.R. § 1.52(d).

☒ English

☐ Non-English

☐ The attached translation includes a statement that the translation is accurate. 37 C.F.R. § 1.52(d).

8. Assignment

☒ An assignment of the invention to Nokia Mobile Phones Ltd.

☒ is attached. A separate ☒ "COVER SHEET FOR ASSIGNMENT (DOCUMENT) ACCOMPANYING NEW PATENT APPLICATION" or ☐ FORM PTO 1595 is also attached.

☐ will follow.

NOTE: "If an assignment is submitted with a new application, send two separate letters-one for the application and one for the assignment." Notice of May 4, 1990 (1114 O.G. 77-78).

WARNING: *A newly executed "CERTIFICATE UNDER 37 C.F.R. § 3.73(b)" must be filed when a continuation-in-part application is filed by an assignee. Notice of April 30, 1993, 1150 O.G. 62-64.*

9. Certified Copy

Certified copy(ies) of application(s)

Country	Appln. No.	Filed
Finland	990038	11 January 1999
Country	Appln. No.	Filed
Country	Appln. No.	Filed

from which priority is claimed

☒ is (are) attached.

☐ will follow.

NOTE: The foreign application forming the basis for the claim for priority must be referred to in the oath or declaration. 37 C.F.R. § 1.55(a) and 1.63.

NOTE: This item is for any foreign priority for which the application being filed directly relates. If any parent U.S. application or International Application from which this application claims benefit under 35 U.S.C. § 120 is itself entitled to priority from a prior foreign application, then complete Item 18 on the ADDED PAGES FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF PRIOR U.S. APPLICATION(S) CLAIMED.

10. Fee Calculation (37 C.F.R. § 1.16)

A. ☒ Regular application

CLAIMS AS FILED				
	Number filed	Number Extra	Rate	Basic Fee 37 C.F.R. § 1.16(a) $ 690.00
Total Claims (37 C.F.R. § 1.16(c))	7	− 20 = 0	× $ 18.00	0
Independent Claims (37 C.F.R. § 1.16(b))	2	− 3 = 0	× $ 78.00	0
Multiple dependent claim(s), if any (37 C.F.R. § 1.16(d))			+ $260.00	

☐ Amendment cancelling extra claims is enclosed.

☒ Amendment deleting multiple-dependencies is enclosed.

☐ Fee for extra claims is not being paid at this time.

NOTE: If the fees for extra claims are not paid on filing they must be paid or the claims cancelled by amendment, prior to the expiration of the time period set for response by the Patent and Trademark Office in any notice of fee deficiency. 37 C.F.R. § 1.16(d).

Filing Fee Calculation $ 690.00

B. ☐ Design application ($310.00—37 C.F.R. § 1.16(f))

Filing Fee Calculation $_____

C. ☐ Plant application ($480.00—37 C.F.R. § 1.16(g))

Filing fee calculation $_____

11. Small Entity Statement(s)

☐ Statement(s) that this is a filing by a small entity under 37 C.F.R. § 1.9 and 1.27 is (are) attached.

WARNING: *"Status as a small entity must be specifically established in each application or patent in which the status is available and desired. Status as a small entity in one application or patent does not affect any other application or patent, including applications or patents which are directly or indirectly dependent upon the application or patent in which the status has been established. The refiling of an application under § 1.53 as a continuation, division, or continuation-in-part (including a continued prosecution application under § 1.53(d)), or the filing of a reissue application requires a new determination as to continued entitlement to small entity status for the continuing or reissue application. A nonprovisional application claiming benefit under 35 U.S.C. § 119(e), 120, 121, or 365(c) of a prior application, or a reissue application may rely on a statement filed in the prior application or in the patent if the nonprovisional application or the reissue application includes a reference to the statement in the prior application or in the patent or includes a copy of the statement in the prior application or in the patent and status as a small entity is still proper and desired. The payment of the small entity basic statutory filing fee will be treated as such a reference for purposes of this section." 37 C.F.R. § 1.28(a)(2).*

WARNING: *"Small entity status must not be established when the person or persons signing the . . . statement can unequivocally make the required self-certification." M.P.E.P., § 509.03, 6th ed., rev. 2, July 1996 (emphasis added).*

(complete the following, if applicable)

☐ Status as a small entity was claimed in prior application

_____ / _____, filed on _____, from which benefit is being claimed for this application under:

35 U.S.C. § ☐ 119(e),
☐ 120,
☐ 121,
☐ 365(c),

and which status as a small entity is still proper and desired.

☐ A copy of the statement in the prior application is included.

Filing Fee Calculation (50% of **A, B** or **C** above)

$_____

NOTE: Any excess of the full fee paid will be refunded if small entitiy status is established and a refund request are filed within 2 months of the date of timely payment of a full fee. The two-month period is not extendable under § 1.136. 37 C.F.R. § 1.28(a).

12. Request for International-Type Search (37 C.F.R. § 1.104(d))

(complete, if applicable)

☐ Please prepare an international-type search report for this application at the time when national examination on the merits takes place.

13. Fee Payment Being Made at This Time

☐ Not Enclosed

☐ No filing fee is to be paid at this time.
(This and the surcharge required by 37 C.F.R. § 1.16(e) can be paid subsequently.)

☒ Enclosed

☒ Filing fee $ 690.00

☒ Recording assignment
($40.00; 37 C.F.R. § 1.21(h))
(See attached "COVER SHEET FOR ASSIGNMENT ACCOMPANYING NEW APPLICATION".) $ 40.00

☐ Petition fee for filing by other than all the inventors or person on behalf of the inventor where inventor refused to sign or cannot be reached
($130.00; 37 C.F.R. §§ 1.47 and 1.17(i)) $ _____

☐ For processing an application with a specification in a non-English language
($130.00; 37 C.F.R. §§ 1.52(d) and 1.17(k)) $ _____

☐ Processing and retention fee
($130.00; 37 C.F.R. §§ 1.53(d) and 1.21(l)) $ _____

☐ Fee for international-type search report
($40.00; 37 C.F.R. § 1.21(e)) $ _____

NOTE: 37 C.F.R. § 1.21(l) establishes a fee for processing and retaining any application that is abandoned for failing to complete the application pursuant to 37 C.F.R. § 1.53(f) and this, as well as the changes to 37 C.F.R. §§ 1.53 and 1.78(a)(1), indicate that in order to obtain the benefit of a prior U.S. application, either the basic filing fee must be paid, or the processing and retention fee of § 1.21(l) must be paid, within 1 year from notification under § 53(f).

Total fees enclosed $ 730.00

14. Method of Payment of Fees

☒ Check in the amount of $ 730.00

☐ Charge Account No. _____ in the amount of $_____.

A duplicate of this transmittal is attached.

NOTE: Fees should be itemized in such a manner that it is clear for which purpose the fees are paid. 37 C.F.R. § 1.22(b).

15. Authorization to Charge Additional Fees

WARNING: *If no fees are to be paid on filing, the following items should not be completed.*

WARNING: *Accurately count claims, especially multiple dependent claims, to avoid unexpected high charges, if extra claim charges are authorized.*

☒ The Commissioner is hereby authorized to charge the following additional fees by this paper and during the entire pendency of this application to Account No. 16-1350 :

☒ 37 C.F.R. § 1.16(a), (f) or (g) (filing fees)

☒ 37 C.F.R. § 1.16(b), (c) and (d) (presentation of extra claims)

NOTE: Because additional fees for excess or multiple dependent claims not paid on filing or on later presentation must only be paid or these claims cancelled by amendment prior to the expiration of the time period set for response by the PTO in any notice of fee deficiency (37 C.F.R. § 1.16(d)), it might be best not to authorize the PTO to charge additional claim fees, except possibly when dealing with amendments after final action.

☒ 37 C.F.R. § 1.16(e) (surcharge for filing the basic filing fee and/or declaration on a date later than the filing date of the application)

☒ 37 C.F.R. § 1.17(a)(1)–(5) (extension fees pursuant to § 1.136(a)).

☐ 37 C.F.R. § 1.17 (application processing fees)

NOTE: ". . .A written request may be submitted in an application that is an authorization to treat any concurrent or future reply, requiring a petition for an extension of time under this paragraph for its timely submission, as incorporating a petition for extension of time for the appropriate length of time. An authorization to charge all required fees, fees under § 1.17, or all required extension of time fees will be treated as a constructive petition for an extension of time in any concurrent or future reply requiring a petition for an extension of time under this paragraph for its timely submission. Submission of the fee set forth in § 1.17(a) will also be treated as a constructive petition for an extension of time in any concurrent reply requiring a petition for an extension of time under this paragraph for its timely submission." 37 C.F.R. § 1.136(a)(3).

☐ 37 C.F.R. § 1.18 (issue fee at or before mailing of Notice of Allowance, pursuant to 37 C.F.R. § 1.311(b))

NOTE: Where an authorization to charge the issue fee to a deposit account has been filed before the mailing of a Notice of Allowance, the issue fee will be automatically charged to the deposit account at the time of mailing the notice of allowance. 37 C.F.R. § 1.311(b).

NOTE: 37 C.F.R. § 1.28(b) requires "Notification of any change in status resulting in loss of entitlement to small entity status must be filed in the application . . . prior to paying, or at the time of paying, . . . the issue fee. . . " From the wording of 37 C.F.R. § 1.28(b), (a) notification of change of status must be made even if the fee is paid as "other than a small entity" and (b) no notification is required if the change is to another small entity.

16. Instructions as to Overpayment

NOTE: ". . . Amounts of twenty-five dollars or less will not be returned unless specifically requested within a reasonable time, nor will the payer be notified of such amounts; amounts over twenty-five dollars may be returned by check or, if requested, by credit to a deposit account." 37 C.F.R. § 1.26(a).

☒ Credit Account No. 16-1350

☐ Refund

SEND ALL CORRESPONDENCE TO:

SIGNATURE OF PRACTITIONER

Reg. No. 24,622

Clarence A. Green

(type or print name of attorney)

Tel. No. (203) 259-1800

PERMAN & GREEN, LLP

P.O. Address

Customer No.

425 Post Road, Fairfield, Connecticut 06430

☐ **Incorporation by reference of added pages**

(check the following item if the application in this transmittal claims the benefit of prior U.S. application(s) (including an international application entering the U.S. stage as a continuation, divisional or C-I-P application) and complete and attach the ADDED PAGES FOR NEW APPLICATION TRANSMITTAL WHERE BENEFIT OF PRIOR U.S. APPLICATION(S) CLAIMED)

☐ Plus Added Pages for New Application Transmittal Where Benefit of Prior U.S. Application(s) Claimed

Number of pages added _____

☐ Plus Added Pages for Papers Referred to in Item 4 Above

Number of pages added _____

☐ Plus added pages deleting names of inventor(s) named in prior application(s) who is/are no longer inventor(s) of the subject matter claimed in this application.

Number of pages added _____

☐ Plus "Assignment Cover Letter Accompanying New Application"

Number of pages added _____

☒ **Statement Where No Further Pages Added**

(if no further pages form a part of this Transmittal, then end this Transmittal with this page and check the following item)

☒ This transmittal ends with this page.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Express Mail No.: EL067144474US

In re Application of: AHO et al.

SERIAL NUMBER: EXAMINER:

FILING DATE: Herewith ART UNIT:

TITLE: METHOD FOR REFRESHING A DYNAMIC MEMORY

ATTORNEY DOCKET NO.: 460-009131-US(PAR)

The Commissioner of Patents and Trademarks

Washington, D.C. 20231

PRELIMINARY AMENDMENT

Dear Sir:

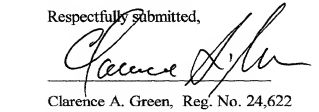
Please amend the above-identified, enclosed patent application as follows:

IN THE CLAIMS:

Please amend Claim 7 as shown below.

Claim 7, line 1, delete "5 or 6,".

Respectfully submitted,



11 Jan 00

Clarence A. Green, Reg. No. 24,622 Date

Perman & Green, LLP

425 Post Road

Fairfield, CT 06430

(203) 259-1800

Method for refreshing a dynamic memory

The invention relates to a method for refreshing memory cells in a dynamic memory, which memory cells are used for storing information, wherein the refreshing is conducted in order to maintain the information in the memory cells, the information stored in the memory cells at a given time is divided into information to be maintained and information not requiring maintenance, wherein at least some of such memory cells which contain information not requiring maintenance, remain unrefreshed, in which method application programs are executed. The invention also relates to an electronic device which comprises a dynamic memory containing memory cells for storing information, means for refreshing the memory cells, means for executing application programs, means for allocating a memory area from the dynamic memory for each application program for the duration of its execution, and means for deallocating said memory area after the execution of the application program.

Especially for temporary storage of data, random access memories (RAM), such as static random access memories (SRAM) and dynamic random access memories (DRAM), are used e.g. for the reason that they enable relatively fast reading and writing of data when compared with other rewritable memory types, such as the non-volatile random access memory (NVRAM).

In memory cells of static memories, the data written therein is maintained when a voltage is coupled to the memory, but in dynamic memories, the data written in the memory cells must be refreshed at regular intervals in order to maintain the data. In static memories, the memory cell is typically formed of several CMOS transistors, or the like. In dynamic memories, the memory cell typically comprises one CMOS transistor and a capacitor. Thus, the memory cell of a dynamic memory requires a smaller surface area and is less expensive than the memory cell of a static memory. Therefore, dynamic memories are used especially in applications requiring a large memory capacity. In the memory cells of the dynamic memory, a charge stored in the capacitance gradually fades away e.g. due to leakage currents. Thus, the memories have to be provided with means for maintaining

(refreshing) the data (charge) stored in the memory cells at intervals. This increases the power consumption of the electronic device when compared with a situation where static memories are used as random access memories.

Especially in portable electronic devices, the aim is to minimize this power consumption in order to prolong the operating time of the device. The power consumption of the memory has not, however, been a significant drawback, because the memory quantity has been relatively small and a large share of the power consumption has been caused by other functions of the electronic device.

Lately, however, the features of portable electronic devices, such as communication devices have been developed, and the quantity of random access memory has been significantly increased. This is because e.g. the applications used in such portable electronic devices require more efficiency and memory capacity than before. The use of the static memory in such applications is restricted by the relatively high price of the static memory. Another restricting factor for the use of the static memory is the large size it requires, wherein the size of the device should be increased in order to implement the necessary memory capacity in the electronic device. However, the aim is to further reduce the size of portable electronic devices, and thus to use the dynamic memory as a random access memory.

There are primarily two types of dynamic memories, an asynchronous dynamic memory (DRAM) and a synchronous dynamic memory (SDRAM). Furthermore, there may be differences in the internal structures of memories of the same basic type, for example as regards the organization of the memory cells, cache memory, and a possible division into blocks (bank). The difference between asynchronous and synchronous memories lies primarily in the fact that in synchronous DRAM memories, data is written in bursts and in a synchronous manner controlled by a clock signal. In asynchronous and synchronous DRAM memories, the memory cells are organized in a matrix format, wherein the memory is provided with a control logic by means of which it is possible to indicate each memory cell of the matrix. The control logic comprises means for indicating a matrix row and means for

indicating a matrix column. The address is typically transmitted in two phases in such a way that in the first phase a matrix row address corresponding to the target address is written in the memory and in the second phase a matrix column address is written in the memory. From these row and column addresses, the control logic of the memory produces a signal to indicate the correct memory cell in the matrix. Typically, these different row and column addresses are written on the same address lines with the difference that when writing the row address, the memory is informed of the row address in question by means of a separate row address strobe line (RAS), and correspondingly, when writing the column address, the memory is informed of the column address in question by means of a separate column address strobe line (CAS).

In an electronic device, the width of the data bus typically equals the width of a byte (8 bits), or its multiple (16, 32 bits). This can be implemented either in such a way that each bit is provided with one or more dynamic memory circuits (parallel coupling of the memory circuits), or that dynamic memory circuits are used which contain several memory matrices integrated therein, for example 8 matrices in parallel. These dynamic memories can also be implemented in such a way that they are integrated in connection with so-called ASIC circuits as is known by anyone skilled in the art.

In dynamic memory circuits of prior art, the refreshing of the memory is arranged in such a way that a memory refresh logic refreshes the memory at intervals, advantageously in such a way that the memory refresh logic indicates each matrix row at a time, reads the information content of this matrix row into an intermediate buffer and writes it back into this matrix row. The refresh logic goes through each matrix row and performs the aforementioned refresh procedures. The refreshing can be conducted either in a continuous manner or between other read/write operations, in such a way, however, that the maximum refresh sequence allowed is not exceeded in any memory cell of the matrix.

There are also known dynamic memories which are provided with a so-called self refresh function, wherein an external memory refresh

controller initiates a self refresh function for the dynamic memory. Thus, an internal timer of the memory updates a refresh counter which is used to maintain information on the memory area (memory row) to be refreshed at a time. With respect to retaining data, it is important to refresh each memory cell sufficiently often in the self refresh function as well.

Especially for portable electronic devices, different functions for attaining savings in power consumption have been developed to obtain a longer operating time for the electronic device. There can be several such power down modes, and the savings in the power consumption attained thereby can vary. Such power down modes include for instance an idle state and a standby state. In these different power down modes, only some of the functions of the electronic device are active. For example the micro processing unit (MPU) of the electronic device does not execute a program code but waits for an activation strobe from the timer. In the power down mode it is, however, necessary to refresh the dynamic memories. If the memory refresh is implemented with a controller separate from the memories, this memory controller has to function also in the different power down modes. If memories including a refresh logic are used as a dynamic memory, the refresh logic has to function also in the different power down modes. Thus, the refresh functions of the dynamic memories form a major part of the power consumption in these power down modes. This problem becomes even worse, because the need for fast random access memory is increased in new electronic devices. Some dynamic memories have the possibility of setting the memory into a power down mode but the maximum duration of this power down mode at a time is restricted to the length of the refresh sequence, after which the memory has to be reset into a normal mode for the duration of the refreshing.

One purpose of the present invention is to reduce the power consumption of dynamic memories especially in situations when the electronic device is in a power down mode. The invention is based on the idea that the dynamic memory is divided into blocks which can be refreshed irrespective of each other, information on the location of each application program to be executed is stored, as well as on the quantity of memory allocated by each application program to be executed, and

that it is determined which of memory blocks contains information requiring maintenance, wherein the memory refresh is conducted primarily in those blocks which contain information that has to remain unaltered. The method according to the present invention is primarily characterized in what will be presented in the characterizing part of the appended claim 1. The electronic device according to the present invention is characterized in that the electronic device also comprises means for dividing the memory cells into two or more blocks, means for refreshing each block substantially irrespective of each other, and means for defining the need to maintain the information to be stored at a given time, wherein information on the need to maintain the information to be stored in the memory cells at a given time is arranged to be defined at least partly on the basis of the storage locations allocated for the application programs, and that the means for refreshing the memory cells comprise means for determining on the basis of said stored information which of said memory blocks contains information requiring maintenance, wherein other memory blocks are arranged to remain unrefreshed.

With the present invention, significant advantages are achieved when compared with solutions of prior art. With the method according to the invention it is possible to reduce the power consumption of dynamic memories significantly without affecting the rate or other corresponding functional parameters of the dynamic memory. Especially in power down modes, the power consumption of electronic devices utilizing the memory according to the invention can be maintained on a considerably lower level when compared to using memories of prior art, wherein the operating time of such electronic devices is increased, which is especially advantageous in portable electronic devices. In addition to the increased operating time, it is also possible to avoid using a battery of higher capacity. Thus in the electronic device, it is possible to avoid the increase in size and weight caused by a larger and heavier power supply. The invention also enables reducing the power supply, if thereis no need to increase the operating time but it can be maintained on its current level. This enables reducing the size of the electronic device in some cases.

In the following, the present invention will be described in detail with reference to the appended drawings in which

Fig. 1 shows a dynamic memory according to a preferred embodiment of the invention and a control logic of the same in a reduced block diagram, and

Fig. 2 shows an electronic device according to a preferred embodiment of the invention.

Fig. 1 is a reduced block diagram showing the structure of a dynamic memory 1 according to a preferred embodiment of the invention, as well as an interface bus 2 needed in its control and a memory controller 3. In this embodiment, the memory controller 3 is implemented in connection with a processor 4 (Fig. 2), but the invention can also be applied in such electronic devices in which the memory controller 3 is implemented as a separate unit or integrated in connection with the memories 1. Furthermore, it is obvious that at least part of the dynamic memory 1, the interface bus 2, the memory controller 3, and the processor 4 can also be implemented so that they are integrated in an ASIC circuit.

In the dynamic memory 1 according to the invention, the memory cells are divided into blocks 5a—5d, in which the memory cells are advantageously organized in a matrix format, as is known as such. The dynamic memory 1 also comprises a command decoder 6 in which a control logic 7 is controlled on the basis of control signals passing through the interface bus 2. The dynamic memory 1 also comprises a mode selection register 8, a column address buffer 9, a row address buffer 10, a data control block 11, a latch 12, and a data buffer 13. Furthermore, the memory blocks 5a—5d are provided with a row selector 14, a column selector 15 and an amplifier 16. It is obvious that the division of memory cells into the four blocks 5a—5d only provides an example here, and within the scope of the invention, in practical embodiments, the number of the blocks can be different from that presented herein. It should also be mentioned that the row selectors 14,

the column selectors 15 and the amplifiers 16 are arranged separately for each memory block 5a—5d.

The dynamic memory 1 has to be provided with operational parameters in connection with the start-up. This is conducted by programming the desired operational parameters into the mode selection register 8. In order to program the mode selection register in the dynamic memory 1 according to this example, the memory controller 3 sets a chip select line CS, address strobe lines RAS, CAS and a write enable line WE in the interface into an active mode. In this example, said lines are active in a low state, and thus the lines CS, RAS, CAS, WE are set in the logical 0 state. The operational parameters are transmitted to the mode selection register 8 via an address bus in which one or more address bus lines are allocated for each parameter for the purpose of transmitting the value of the parameter. Thus, when setting the aforementioned lines, the memory controller 3 also sets the values corresponding to the desired operating mode, for example a CAS latency and the length of the burst in a burst-nocle transfer, into the bits of the address bus. The CAS latency is used to indicate the time passed in the process of reading the data from the memory, from the act of writing a reading command in the memory 1 to the moment when it can be read in the data bus. The CAS latency time is reported in clock sequences, for example 1, 2 or 3 clock sequences, depending on the speed of the memory and on the frequency of the clock signal. The mode selection register is programmed for example in the ascending edge of the clock signal when the lines CS, RAS, CAS, WE are in the active state. The above-described programming of the mode selection register 8 has to be conducted also when an operational parameter is changed, which is known as such.

In order to address the dynamic memory 1, the memory controller 3 sets the circuit selecting line CS into an active state, which in this embodiment means a voltage rating corresponding to the logical 0 state, in practice approximately 0 V. In case of an operation of writing into the memory 1, the write enable line WE is set in an active state for the duration of the writing operation. If the address bus contains an address corresponding to the row address, the memory controller 3 sets the row address strobe line RAS indicating this row address into

an active state. Thus the command decoder 6 interprets the command in question as a writing command and the address as a row address. The command decoder 6 establishes a control for the control logic 7, which produces a strobe signal for the row address buffer 10, to transfer the row address from the address bus to the output of the row address buffer 10, wherein the address is transmitted to the row selectors 14a—14d. At the next stage, the memory controller 3 sets the column address to the address bus and the corresponding column address strobe line CAS into an active state. Before that, the memory controller 3 has set the row address strobe line RAS into a non-active state (e.g. logical 1 state). Correspondingly, the column address is transmitted via the column address buffer 9 to column selectors 15a—15d. The memory controller 3 also sets the data to be written in the storage location indicated in the data bus, which data is transmitted via the latch 12 to the data control block 11 and further to the memory matrix. The control logic 7 is responsible for selecting the correct block 5a—5d and for establishing timings for the address buffers 9, 10, for the data control block 11 and for the latch 12.

The row address buffer 10 of the dynamic memory is advantageously provided with a referesh counter which is used to conduct a self refresh procedure when no data is written in or read from the dynamic memory 1. The self refresh procedure is controlled by means of the control logic 7 and the mode selection register 8 for example in such a way that the control logic 7 examines the mode selection register 8 to find out which blocks require refreshing and selects such blocks to be refreshed at intervals. The address (row address) of the refresh location is obtained from the refresh counter, which is advantageously increased by one after each refresh operation. Thus the next self refresh procedure is conducted for the following row.

When utilizing burst nocle, the initial address is written from the memory controller 3 to the dynamic memory 1. The column address buffer 9 of the dynamic memory is provided with a column address counter, which is used in burst nocle to select the correct column address at a given time. The data transfer and the stepping of the column address counter are synchronized with the clock signal.

The following is a description on the function of the dynamic memory 1 according to a preferred embodiment of the invention shown in Fig. 1. As an example, it is presumed that the dynamic memory contains 64 Mbit (megabits) of memory organized into words of 16 bits in width, i.e. approximately four million words, and that these words are divided into four blocks 5a—5d. Thus, each block comprises 1 048 576 x 16 memory cells. Consequently, two block selecting lines BA0, BA1 are required for selecting the block, as well as 20 bits for indicating the words in the block. In an advantageous dynamic memory, the coding for indicating the words is arranged in a multiplexed manner in such a way that twelve address lines of the address bus AD, advantageously the lines AD0—AD11, are used to define the row address, and eight address lines, advantageously the lines AD0—AD8, are used to define the column address. For the sake of clarity, in the appended figures these lines of the address bus AD are not shown separately, but as a single bus. It is obvious that the address bus AD can contain a larger number of lines than the lines AD0—AD11 mentioned in this example, but that is not significant for understanding the invention.

Furthermore, to control the dynamic memory 1 according to a preferred embodiment of the invention, two address strobe lines RAS, CAS, and one clock line CLK are used, as well as a clock enable line CKE, by means of which the coupling of the clock signal to the dynamic memory can be controlled.

Data is written advantageously in the following way. The starting address of the desired writing point in the dynamic memory 1 is set for example in two phases in the addres bus AD; first the row address and then the column address, or vice versa. The block is selected with a block selecting command, in connection with which block selecting information is transmitted in these block selecting lines BA0, BA1. At the same time, a row address is advantageously also transmitted. Thus, the row address and the block selecting information is transmitted by the row address strobe line RAS. Correspondingly, the column address is transmitted to the column address buffer by the column address strobe line CAS. The address is formulated for example in such a way that the most significant part of the starting address of the writing point (marked b0—b19), for example the bits

b8—b19, are set as a row address, in such a way that b8 is set to be the value for the least significant bit AD0 of the address bus, b9 is set to be the value for the next least significant bit AD1 of the address bus, etc. The least significant part in the starting address of the writing point, in this case bits b0—b7, is set as a column address advantageously in such a way that b0 is set to be the value of the least significant bit AD0 of the address bus, b1 is set to be the next least significant bit AD1 of the address bus, etc. Furthermore, the memory controller 3 sets the chip select line CS of the dynamic memory 1 to which the memory operation is directed, into an active state.

From the row address buffer 10, the address information is transmitted to the row selector 14a—14d, whereby a memory cell row corresponding to the target area is selected from the memory matrix 5a—5d. Correspondingly, from the column address buffer 9, the address is transmitted to the column selector 15a—15d, which selects the corresponding column from the memory matrix 5a—5d. At the next stage, the data to be stored in the dynamic memory 1 is set to the data bus D.

In this context, it should be mentioned that for the sake of clarity, the lines D0—D15 of the data bus D are not marked separately in the appended figures, but are shown in a single bus. It is obvious that the data bus D can contain a different number of lines than the 16 used in this example.

The clock signal is transmitted to the control logic 7 via the clock line CLK. This clock line is also used for processing most of the internal timings of the dynamic memory 1. The control logic 7 provides the data buffer 13 with control signals to determine the transfer direction of the data in the data buffer 13 (read/write). When writing the data, the direction from the data bus D to the memory matrix 5a—5d is set as a direction data, wherein data is transmitted to the memory matrix 5a—5d for example on the ascending or descending edge of the clock signal. In practice, the data buffer 13 is composed of two separate bus buffers with opposite directions, both buffers being provided with a so-called three-condition output. Such a three-condition output can be set in a

floating position when the output is not active. This enables using the same data bus D for both writing and reading, which is known as such.

Also from the dynamic memory 1 data is read primarily by following the above-presented principles. The most substantial difference is that the state of the read/write line WE is set to another state, in this example to the logical 1 state, which causes the transfer direction of the data to be reversed in the data buffer 13 when compared with the situation of writing the data. When the address data is transmitted to the row selector 14a—14d and to the column selector 15a—15d, the control logic 7 is used to control the data transmission from the memory matrix 5a—5d to the output of the data buffer 13, wherein data can be read from the data bus D. Data is read for example on the descending edge of the clock signal.

The present invention can be advantageously applied in connection with the dynamic memory 1 for example in such a way that the refreshing of each memory block 5a—5d can be controlled separately. Thus, data on those memory blocks 5a—5d which at a given time contain data to be retained, is written for example in the mode selection register. Such memory blocks are refreshed in a conventional manner. However, memory blocks which do not contain information to be retained, are not subjected to refresh procedures. This alternative is suitable for such dynamic memories which are provided with means for conducting the refreshing, wherein an external refresh logic is not necessary.

In a second preferred embodiment of the invention, a dynamic memory 1 is refreshed in connection with the memory controller 3. Thus, the memory controller 3 contains data indicating which memory areas include information which does not have to be retained. Such areas can be left unrefreshed, if they have such a size and location in the dynamic memory 1 that the refresh logic is able to distinguish these areas. In practical applications, it is not reasonable to implement refresh operation according to the invention in such a way that each memory cell can be refreshed or left unrefreshed, but the memory cells are treated in larger entities, for example in rows, or blocks composed of several rows.

Fig. 2 is a reduced block diagram showing an electronic device 17, in connection with which the invention can be advantageously applied. In this example, the electronic device 17 is a communication device comprising data processing functions and mobile station functions. A major part of the functions of the electronic device 17 is implemented in a first ASIC circuit 19. This first ASIC circuit 19 comprises for instance a first processor 4a which is advantageously a so-called general purpose RISC processor, i.e. reduced instruction set computer. Furthermore, the first ASIC circuit 19 comprises a second processor 4b, i.e. a digital signal processor (DSP), in which signal processing functions are typically implemented. The first ASIC circuit 19 also comprises memory means MEM which can be partly shared by the first 4a and the second processor 4b, logic couplings LOGIC, and an interface logic I/O. The couplings between these different blocks of the ASIC circuit 19 are not shown in detail in Fig. 2, because they are prior art known as such by anyone skilled in the art. Fig. 2 shows one further block of the first ASIC circuit 19, i.e. a so-called cache memory CACHE, which is used in connection with the invention, especially in connection with the external dynamic memory 1 in a way described hereinbelow. Furthermore, the electronic device 17 can also comprise other external memory means, such as a FLASH memory.

To the first ASIC circuit 19, a keyboard 21 is coupled, which in this embodiment is a keyboard used primarily in connection with data processing functions, advantageously a so-called QWERTY keyboard. A keypad 22, used primarily in mobile station functions, is also coupled to this first ASIC circuit. In this embodiment, the electronic device 17 also comprises two display devices 23a, 24a, which are controlled by display drivers 23b, 24b. The first display device 23a is primarily used in connection with data processing functions, and the second display device 24a is primarily used in connection with mobile station functions. It is obvious that said keyboard 21 and keypad 22, and the first display device 23a and the second display device 24a can be used in connection with both mobile station functions and data processing functions, if necessary. A microphone 25 and a receiver 26 are coupled via an audio block 27 to the first ASIC circuit 19. This audio block 27 contains a codec, by means of which, for instance during an audio call,

a microphone signal is converted to a digital signal, and the digital speech signal is converted to an analog signal to be transmitted to the receiver 26. The electronic device 17 advantageously also comprises a speaker 28, to which the audio signal is transmitted advantageously via an audio amplifier 29. The speaker 28 is primarily used when the electronic device 17 is for example on a table in a position in which it is possible to use the data processing functions, or in a situation when a call is to be heard by several people nearby, or in a hands-free mode in a vehicle.

The electronic device 17 of Fig. 2 also comprises a high frequency section 30 (RF, Radio Frequency), by means of which calls are transmitted between the electronic device 17 and a mobile communication network (not shown) in a way known as such.

Furthermore, the electronic device 17 comprises a power supply circuit 31, which in this embodiment is also implemented as an ASIC circuit. This power supply circuit 31 comprises means for generating operating voltages V_{CC1}, V_{CC2} from a supply voltage V_{IN}. The supply voltage V_{IN} is advatageously generated by means of a battery 32, which is loaded with a loading device 33 when necessary.

In Fig. 2, the interface between the dynamic memory 1 and the first ASIC circuit 19 is marked as a single bus 2. The dynamic memory 1 is composed of memory cells organized in matrix format in one or more blocks and illustrated by blocks 5a—5d in Fig. 1.

To control the functions of the electronic device 17, the electronic device 17 is provided with one or more operating systems, or the like, which contain functions for controlling the functional units of the electronic device 17, and possibly means for executing different application programs, or the like. The operating system is composed of a group of program commands of the processors, which commands are executed by the processor 4a, 4b. In multiprocessing operating systems, there may be several application programs under execution simultaneously. Thus, the operating system takes care of the execution turns of the different application programs, memory allocations, signal transmission between the functional blocks of the electronic device,

e.g. transmitting the keystrokes to the correct application program, etc. These operating system functions are known as such by anyone skilled in the art.

When starting the application program, its program code is either executed from the program memory or transmitted to the random access memory, for example to the dynamic memory 1. Furthermore, a space is allocated for the application program from the dynamic memory to store data temporarily. Also for the operating systems, a dynamic memory is allocated for temporary storing of data. Thus, in different situations, the need for memory can vary considerably. Furthermore, the simultaneous use of several programs can have a significant effect on the quantity of memory allocated at a given time. In the method according to a preferred embodiment of the invention, the processor 4a, 4b stores information on the location of each application program to be executed, as well as on the quantity of memory allocated by the same. On the basis of this information the processor 4a, 4b knows whether there are such memory areas in the dynamic memory 1 which can be left unexecuted. For example, the dynamic memory 1 according to Fig. 1 contains four memory blocks, the refresh procedure being separately controllable in each. Thus, if a memory block does not contain any such memory cells whose information is to be retained, the memory controller 3 is informed of the fact by the processor 4a, 4b. After that the memory controller 3 does not refresh such memory blocks. If a refresh logic is implemented in the dynamic memory 1, the memory controller 3 transmits information on the free memory areas to the dynamic memory 1, for example in the operational parameters of the mode selection register 8. Thus, in the dynamic memory 1, the refresh logic refreshes such blocks which contain information to be retained.

When starting up a new application program, for example when receiving an incoming call in a communication device, the processor allocates a data memory from the dynamic memory 1. The memory allocation is conducted advantageously in such a way that the allocated areas are located substantially successively in the dynamic memory 1. Thus, the free memory also exists in more uniform entities, and therefore it is easier to implement the refreshing and the act of leaving

the refreshing unexecuted. When the call is finished, the memory area allocated for the telephone application is deallocated, wherein this area does not have to be refreshed any more.

During a call, the data processing functions are not necessarily used, and thus it is not necessary to refresh the memory area allocated for the data processing functions, or it can be utilized by the telephone application if necessary.

It is obvious that the present invention is not restricted solely to the embodiments presented above, but it can be modified within the scope of the appended claims.

Claims:

1. A method for refreshing memory cells in a dynamic memory (1), which memory cells are used for storing information, wherein the refreshing is conducted in order to maintain the information in the memory cells, the information stored in the memory cells at a given time is divided into information to be maintained and information not requiring maintenance, wherein at least some of such memory cells which contain information not requiring maintenance, remain unrefreshed, in which method application programs are executed, **characterized** in that the memory cells of the dynamic memory (1) are divided into two or more blocks (5a, 5b, 5c, 5d) which can be refreshed irrespective of each other, that information on the location of each application program to be executed is stored, as well as on the quantity of memory allocated by each application program to be executed, and that it is determined on the basis of said stored information which of said memory blocks (5a, 5b, 5c, 5d) contains information requiring maintenance, wherein other memory blocks (5a, 5b, 5c, 5d) remains unrefreshed.

2. The method according to claim 1, **characterized** in that the dynamic memory (1) is a synchronous dynamic memory.

3. The method according to claim 1, **characterized** in that the dynamic memory (1) is an asynchronous dynamic memory.

4. An electronic device (17) comprising a dynamic memory (1) with memory cells for storing information, means (3, 7, 10) for refreshing the memory cells, means (4a, 4b) for executing application programs, means (4a, 4b) for allocating a memory area from the dynamic memory (1) for each application program for the duration of its execution, and means (4a, 4b) for deallocating said memory area after the execution of the application program, **characterized** in that the electronic device (17) also comprises means (14a—14d; 15a—15d) for dividing the memory cells into two or more blocks (5a—5d), means (3, 7, 8) for refreshing each block (5a—5d) substantially irrespective of each other, and means (4a, 4b) for defining the need to maintain the information to be stored at a given time, wherein information on the need to maintain

the information to be stored in the memory cells at a given time is arranged to be defined at least partly on the basis of the storage locations allocated for the application programs, and that the means for refreshing the memory cells comprise means (3, 4a, 4b, 8) for determining on the basis of said stored information which of said memory blocks (5a, 5b, 5c, 5d) contains information requiring maintenance, wherein other memory blocks (5a, 5b, 5c, 5d) are arranged to remain unrefreshed.

5. The electronic device (17) according to claim 4, **characterized** in that the dynamic memory (1) comprises a synchronous dynamic memory.

6. The electronic device (17) according to claim 4, **characterized** in that the dynamic memory (1) comprises an asynchronous dynamic memory.

7. The electronic device (17) according to claim 4, 5 or 6, **characterized** in that it is a communication device comprising mobile station functions.

Abstract:

The invention relates to a method for refreshing memory cells in a dynamic memory (1), which memory cells are used to store information, wherein the refreshing is conducted in order to maintain information contained in the memory cells. In the memory cells, the information stored therein at a given time is divided into information to be maintained and information not requiring maintenance, wherein at least some of such memory cells containing information not requiring maintenance are left unrefreshed. In the method application programs are executed. The memory cells of the dynamic memory (1) are divided into two or more blocks (5a, 5b, 5c, 5d) which can be refreshed irrespective of each other. Information on the location of each application program to be executed is stored, as well as on the quantity of memory allocated by each application program to be executed. In the method it is further determined on the basis of said stored information which of said memory blocks (5a, 5b, 5c, 5d) contains information requiring maintenance, wherein other memory blocks (5a, 5b, 5c, 5d) remains unrefreshed The invention also relates to an electronic device (17).

Fig. 1

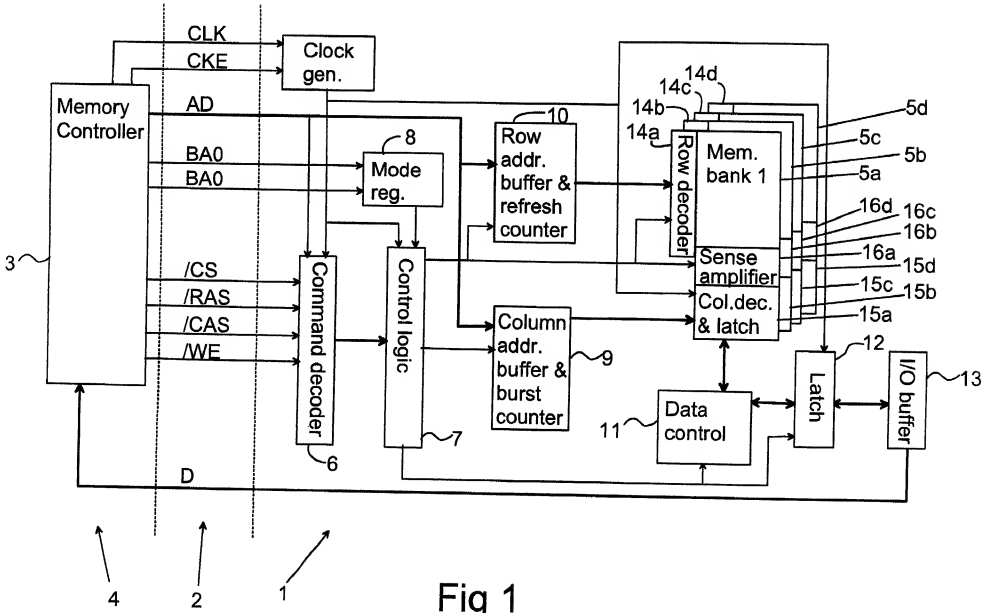


Fig 1

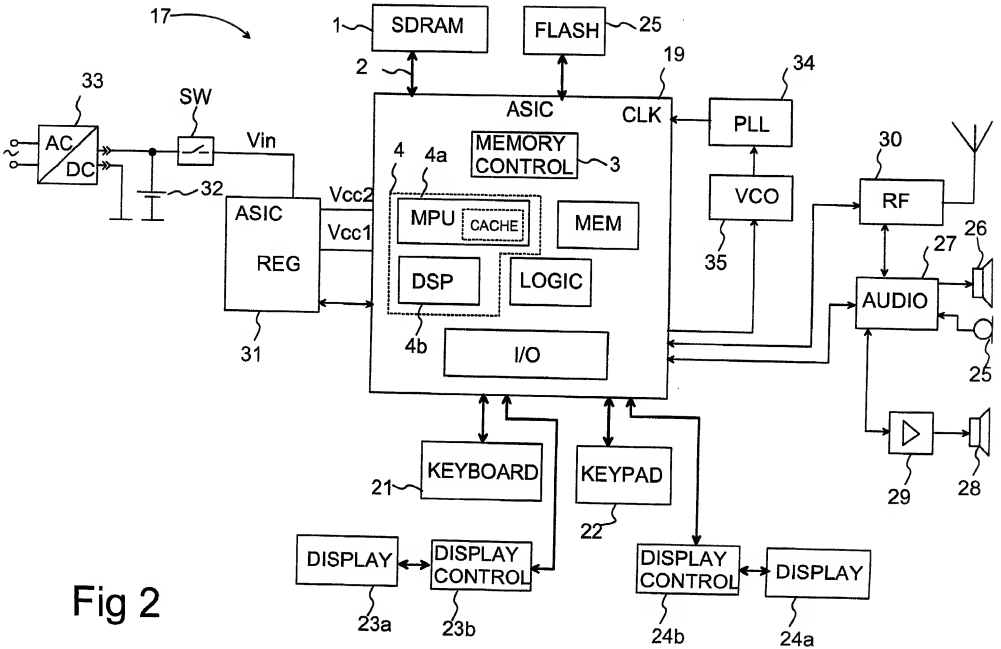


Fig 2

Attorney's Docket No. _____ ***PATENT***

COMBINED DECLARATION AND POWER OF ATTORNEY

(ORIGINAL, DESIGN, NATIONAL STAGE OF PCT, SUPPLEMENTAL, DIVISIONAL, CONTINUATION OR C-I-P)

As a below named inventor, I hereby declare that:

TYPE OF DECLARATION

This declaration is of the following type:

(check one applicable item below)

[x] original.

[ ] design.

[ ] supplemental.

NOTE: *If the declaration is for an International Application being filed as a divisional, continuation or continuation-in-part application, do not check next item; check appropriate one of last three items.*

[ ] national stage of PCT.

NOTE: *If one of the following 3 items apply, then complete and also attach ADDED PAGES FOR DIVISIONAL, CONTINUATION OR C-I-P.*

[ ] divisional.

[ ] continuation.

[ ] continuation-in-part (C-I-P).

INVENTORSHIP IDENTIFICATION

WARNING: *If the inventors are each not the inventors of all the claims, an explanation of the facts, including the ownership of all the claims at the time the last claimed invention was made, should be submitted.*

My residence, post office address and citizenship are as stated below, next to my name. I believe that I am the original, first and sole inventor *(if only one name is listed below)* or an original, first and joint inventor *(if plural names are listed below)* of the subject matter that is claimed, and for which a patent is sought on the invention entitled:

TITLE OF INVENTION

Method for refreshing a dynamic memory

SPECIFICATION IDENTIFICATION

the specification of which:

(complete (a), (b), or (c))

(a) [x] is attached hereto

(b) [ ] was filed on _____ as [ ] Serial No. 0/ _____
or [ ] Express Mail No., As Serial No. not yet known _____
and was amended on _____ *(if applicable).*

NOTE: Amendments filed after the original papers are deposited with the PTO that contain new matter are not accorded a filing date by being referred to in the declaration. Accordingly, the amendments involved are those filed with the application papers or, in the case of a supplemental declaration, are those amendments claiming matter not encompassed in the original statement of invention or claims. See 37 CFR 1.67.

(c) [ ] was described and claimed in PCT International Application No. _____, filed on _____ and as amended under PCT Article 19 on _____ *(if any).*

ACKNOWLEDGEMENT OF REVIEW OF PAPERS AND DUTY OF CANDOR

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information, which is material to patentability as defined in 37, Code of Federal Regulations, § 1.56,

(also check the following items, if desired)

[x] and which is material to the examination of this application, namely, information where there is a substantial likelihood that a reasonable Examiner would consider it important in deciding whether to allow the application to issue as a patent, and

[ ] in compliance with this duty, there is attached an information disclosure statement, in accordance with 37 CFR 1.98.

PRIORITY CLAIM (35 U.S.C § 119(a)–(d))

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)–(d) of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed.

(complete (d) or (e)

(d) [ ] no such applications have been filed.

(e) [x] such applications have been filed as follows.

NOTE: where item (c) is entered above and the International Application which designated the U.S. itself claimed priority check item (e), enter the details below and make the priority claim.

PRIOR FOREIGN/PCT APPLICATION(S) FILED WITHIN 12 MONTHS (6 MONTHS FOR DESIGN) PRIOR TO THIS APPLICATION AND ANY PRIORITY CLAIMS UNDER 35 U.S.C. § 119(a)–(d)

COUNTRY (OR INDICATE IF PCT)	APPLICATION NUMBER	DATE OF FILING (day, **month**, year)	PRIORITY CLAIMED UNDER 37 USC 119
Finland	**990038**	**11 January 1999**	[x] YES NO [ ]
			[ ] YES NO [ ]
			[ ] YES NO [ ]
			[ ] YES NO [ ]
			[ ] YES NO [ ]

CLAIM FOR BENEFIT OF PRIOR U.S. PROVISIONAL APPLICATION(S)
(34 U.S.C. § 119(e))

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below:

PROVISIONAL APPLICATION NUMBER	FILING DATE
/	
/	
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CLAIM FOR BENEFIT OF EARLIER US/PCT APPLICATION(S) UNDER 35 U.S.C. 120

[ ] The claim for the benefit of any such applications are set forth in the attached ADDED PAGES TO COMBINED DECLARATION AND POWER OF ATTORNEY FOR DIVISIONAL, CONTINUATION OR CONTINUATION-IN-PART (C-I-P) APPLICATION

ALL FOREIGN APPLICATION(S), *IF ANY*, FILED MORE THAN 12 MONTHS (6 MONTHS FOR DESIGN) PRIOR TO THIS U.S. APPLICATION

NOTE: If the application filed more than 12 months from the filing date of this application is a PCT filing forming the basis for this application entering the United States as (1) the national stage, or (2) a continuation, divisional, or continuation-in-part, then also complete ADDED PAGES TO COMBINED DECLARATION AND POWER OF ATTORNEY FOR DIVISIONAL, CONTINUATION OR C-I-P APPLICATION for benefit of the prior U.S. or PCT application(s) under 35 U.S.C. § 120.

POWER OF ATTORNEY

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

(list name and registration number)

Clarence A. Green (24,622)
Harry F. Smith (32,493)
Mark F. Harrington (31,686)

(check the following item, if applicable)

☐ Attached, as part of this declaration and power of attorney, is the authorization of the above-named attorney(s) to accept and follow instructions from my representative(s).

SEND CORRESPONDENCE TO

Clarence A. Green
Perman & Green, LLP
425 Post Road
Fairfield, CT 06430

DIRECT TELEPHONE CALLS TO:
(Name and telephone number)
Clarence A. Green
(203) 250–1800

DECLARATION

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

SIGNATURE(S)

NOTE: *Carefully indicate the family (or last) name, as it should appear on the filing receipt and all other documents.*

Full name of sole or first inventor

Matti		Floman
(GIVEN NAME)	(MIDDLE INITIAL OR NAME)	FAMILY (OR LAST NAME)

Inventor's signature 

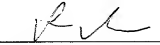
Date 26 October 1999 Country of Citizenship Finland

Residence Ylioppilaankatu 7 A 14, FIN-33720 Tampere, Finland

Post Office Address Ylioppilaankatu 7 A 14, FIN-33720 Tampere, Finland

Full name of second joint inventor, if any

Ari		Aho
(GIVEN NAME)	(MIDDLE INITIAL OR NAME)	FAMILY (OR LAST NAME)

Inventor's signature 

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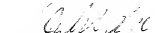
Full name of third joint inventor, if any

Markku		Lipponen
(GIVEN NAME)	MIDDLE INITIAL OR NAME	FAMILY (OR LAST NAME)

Inventor's signature 

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(check proper box(es) for any of the following added page(s) that form a part of this declaration)

☒ **Signature** for fourth and subsequent joint inventors. *Number of pages added* 1

* * *

☐ **Signature** by administrator(trix), executor(trix) or legal representative for deceased or incapacitated inventor. *Number of pages added* _____

* * *

☐ **Signature** for inventor who refuses to sign or cannot be reached by person authorized under 37 CFR 1.47. *Number of pages added* _____

* * *

☐ Added page for **signature** by one joint inventor on behalf of deceased inventor(s) where legal representative cannot be appointed in time. (37 CFR 1.47)

* * *

☐ Added pages to combined declaration and power of attorney for divisional, continuation, or continuation-in-part (C-I-P) application.

☐ Number of pages added _____

* * *

☐ Authorization of attorney(s) to accept and follow instructions from representative.

* * *

(if no further pages form a part of this Declaration, then end this Declaration with this page and check the following item)

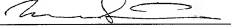
☐ This declaration ends with this page.

SIGNATURE(S)

NOTE: *Carefully indicate the family (or last) name, as it should appear on the filing receipt and all other documents.*

Full name of fourth joint inventor, if any

Mikko		Siltanen
(GIVEN NAME)	(MIDDLE INITIAL OR NAME)	FAMILY (OR LAST NAME)

Inventor's signature 

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Full name of joint inventor, if any

(GIVEN NAME)	(MIDDLE INITIAL OR NAME)	FAMILY (OR LAST NAME)

Inventor's signature

Date Country of Citizenship

Residence

Post Office Address

Full name of joint inventor, if any

(GIVEN NAME)	(MIDDLE INITIAL OR NAME)	FAMILY (OR LAST NAME)

Inventor's signature

Date Country of Citizenship

Residence

Post Office Address